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EXAMINER	
BAND, MICHAEL A	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/799,361	Applicant(s) DOAN ET AL.	
	Examiner MICHAEL BAND	Art Unit 1795	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-24,26-28,30-32,34-36 and 38-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-24, 26-28, 30-32, 34-36, and 38-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-7, 12-14, 18-20, 24, 26-28, 30-32, 34-36, and 38-40 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Vukanovic et al (US Patent No. 4,505,947).

With respect to claims 1 and 12, Vukanovic et al discloses a method for the deposition of coatings upon substrates (i.e. targets) utilizing arc plasma (i.e. electrical arcing) (abstract), where one embodiment of the invention of coated substrates are prepared by establishing electric field conditions in which an arc plasma may exists between a first electrode and a second electrode (col. 2, lines 63-68). Vukanovic et al further discloses that the coating material may be placed on or in a cathode, where it is vaporized by the heat of the cathode and carried into the plasma region by a carrier gas (col. 4, lines 4-9). Vukanovic et al describes how the coating materials are introduced into the region of the electrodes in a condensed state, such as a wire and volatized by the heat generated at or on the cathode (col. 4, lines 15-19) and if conductive (i.e. metal) as a sacrificial (i.e. consumable) cathode (col. 4, lines 19-22). Vukanovic et al lists suitable coating materials as metals (col. 4, lines 25-33). Vukanovic et al also

describes how the plasma material is introduced into the arc plasma and positioning a substrate material proximate to the arc plasma, whereby said coating material formed by the arc plasma contact the substrate to form a coating (col. 3, lines 8-13). It is well known that for a solid to be vaporized, the solid transitions from a solid state to a liquid state, thus the metal is liquefied. Furthermore, Vukanovic et al discusses that “the types and proportions of the materials introduced into the region of the electrodes can be modified during the deposition process in order that discrete or graded layers of p, i and n material (as termed in the art) can be successively deposited, in any order” (col. 4, lines 52-57), thus the process is repeated to form a plurality of metal layers (p, i, and n). Vukanovic et al further discloses that the coating material is deposited onto the surface of the substrate (col. 3, lines 8-13), where the substrate may be a semiconductor (col. 3, lines 14-23). While Vukanovic et al does not suggest the substrate (i.e. used target) have depressions or gaps (i.e. sputtered depressions), it is either inherent or obvious that a semiconductor substrate possess this specified feature as evidenced by Miyazaki (US Patent No. 5,595,938; figs. 1-4) and Lee et al (US Patent No. 7,192,335; figs. 1-2). Furthermore it is well known that a sputter target (i.e. substrate) is eroded unevenly during use, leading to depressions on the target surface.

With respect to claim 3, Vukanovic et al further depicts fig. 4 with an anode and a cathode (i.e. two electrodes) [11], [12], where the cathode is a sacrificial cathode (col. 4, lines 21-22) in the form of a wire (col. 4, lines 15-19). A plasma arc (i.e. electrical arc) exists between a first electrode and a second electrode (col. 2, lines 63-67). The arc current utilized to generate the plasma may be as low as 0.5 amps (col. 5, lines 17-18),

thus the arc is electrical. It is inherent that the sacrificial (i.e. consumable) wire be present when an electrical arc is generated in order to coat the substrate.

With respect to claim 4, Vukanovic et al further discloses introducing a coating material into the arc plasma and positioning the substrate material proximate to the arc plasma, whereby said coating material formed by the arc plasma contact the substrate to form the coating (col. 3, lines 8-13), thus the plasma arc is also in contact with the substrate. Furthermore “the arc current utilized to generate the plasma may be as low as 0.5 amps” (col. 5, lines 17-18), leading to the conclusion that the plasma arc is equivalent to an electrical arc.

With respect to claims 5-7, Vukanovic et al further discloses suitable coating materials for deposition upon substrates include aluminum, copper, and germanium (col. 4, lines 25-33).

With respect to claims 13-14 and 18-19, Vukanovic et al further discloses that “the temperature of the plasma jet which emerges from the exit orifice […] has been measured from 200^{o}C – 700^{o}C” (col. 5, lines 42-44). The exit orifice [44] can be seen in fig. 3 near arc plasma region [16]. Fig. 4 depicts the arc plasma region adjacent to the substrate [43], as also stated (col. 8, lines 28-31). Thus the substrate is in close proximity to the exit orifice with the substrate layers being exposed to an energy source (i.e. the plasma jet heat).

With respect to claim 20, Vukanovic et al further depicts in fig. 3 a magnetic field D.C. source (i.e. electromagnet) [35] contains the arc plasma inside the chamber (col. 9, lines 6-9). The plasma produced by the arc reaches several thousand degrees (col. 9,

lines 17-18), thus being a form of energy. The carrier gas further transports these species (i.e. arc plasma with coating materials) out exit orifice [44] where anything in that vicinity, such as flat substrates may be uniformly coated with the coating material (col. 9, lines 22-27). The plasma that emerges from the exit orifice is a plasma jet (i.e. beam) at a temperature of 200°C – 700°C (col. 5, lines 42-43). As stated earlier, this plasma jet heats the substrate layers to recrystallize them since recrystallized is related to annealing as defined by Wikipedia.com. Therefore the substrate is annealed since it is heated at a temperature of 700°C and cooled at a temperature of 200°C. Thus the substrate is heated by an electromagnetic energy beam.

With respect to claims 24, 28, 32, and 36 Vukanovic et al discloses a method for the deposition of coatings upon substrates (i.e. targets) utilizing arc plasma (i.e. electrical arcing) (abstract), where one embodiment of the invention of coated substrates are prepared by establishing electric field conditions in which an arc plasma may exists between a first electrode and a second electrode (col. 2, lines 63-68). Vukanovic et al further discloses that the coating material may be placed on or in a cathode, where it is vaporized by the heat of the cathode and carried into the plasma region by a carrier gas (col. 4, lines 4-9). Vukanovic et al describes how the coating materials are introduced into the region of the electrodes in a condensed state, such as a wire and volatized by the heat generated at or on the cathode (col. 4, lines 15-19) and if conductive (i.e. metal) as a sacrificial (i.e. consumable) cathode (col. 4, lines 19-22). An arc plasma is generated by impressing a voltage between the cathode (i.e. first electrode) and anode (i.e. second electrode) (col. 6, lines 66-68). Futhermore,

Vukanovic et al discusses introducing a coating material into the arc plasma and positioning the substrate material proximate to the arc plasma, whereby said coating material formed by the arc plasma contact the substrate to form the coating (col. 3, lines 8-13), thus the plasma arc is also in contact with the substrate. Furthermore "the arc current utilized to generate the plasma may be as low as 0.5 amps" (col. 5, lines 17-18), leading to the conclusion that the plasma arc is equivalent to an electrical arc. Fig. 3 depicts an exit orifice (i.e. nozzle) [44] forms a jet stream of plasma exiting the chamber [25]. Vukanovic et al lists suitable coating materials as metals (col. 4, lines 25-33). Vukanovic et al also describes how the plasma material is introduced into the arc plasma and positioning a substrate material proximate to the arc plasma, whereby said coating material formed by the arc plasma contact the substrate to form a coating (col. 3, lines 8-13). It is well known that for a solid to be vaporized, the solid must transition from a solid state to a liquid state, thus the metal is liquefied. Vukanovic et al further discloses that the coating material is deposited onto the surface of the substrate (col. 3, lines 8-13), where the substrate may be a semiconductor (col. 3, lines 14-23). While Vukanovic et al does not suggest the substrate (i.e. used target) have depressions or gaps (i.e. sputtered depressions), it is either inherent or obvious that a semiconductor substrate possess this specified feature as evidenced by Miyazaki (US Patent No. 5,595,938; figs. 1-4) and Lee et al (US Patent No. 7,192,335; figs. 1-2). Furthermore it is well known that a sputter target (i.e. substrate) is eroded unevenly during use, leading to depressions on the target surface.

With respect to claims 26, 30, 34, and 38, Vukanovic et al further discloses suitable coating materials for deposition upon substrates include aluminum, copper, and germanium (col. 4, lines 25-33).

With respect to claims 27, 31, 35, and 39, Vukanovic et al further discloses suitable coating materials, including germanium.

With respect to claim 40, Vukanovic et al further depicts fig. 4 with an anode and a cathode (i.e. two electrodes) [11], [12], where the cathode is a sacrificial cathode (col. 4, lines 21-22) in the form of a wire (col. 4, lines 15-19). A plasma arc (i.e. electrical arc) exists between a first electrode and a second electrode (col. 2, lines 63-67). The arc current utilized to generate the plasma may be as low as 0.5 amps (col. 5, lines 17-18), thus the arc is electrical. It is inherent that the sacrificial (i.e. consumable) wire be present when an electrical arc is generated in order to coat the substrate.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 8-9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vukanovic et al (US Patent No. 4,505,947) as applied to claims 7 and 12.

With respect to claim 8, the reference is cited as discussed for claims 7 and 12. Vukanovic et al further discloses suitable coating materials for deposition upon substrates include silicon and other semiconductor component or dopant materials including aluminum and copper (col. 4, lines 25-33). However Vukanovic et al is limited in that while it describes using these three components for the coating materials, it is not suggested as to the specific compositional percentages of these components.

It has been held that differences in concentration or temperature will not support patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Therefore it would have been obvious to one of ordinary skill in the art to use the coating material composition discussed in Vukanovic et al with various percentage compositions, including those claimed, since one of ordinary skill would expect similar characteristics.

With respect to claim 9, Vukanovic et al further discloses that the coating material may be placed on or in the cathode (col. 4, lines 4-6), such as a sacrificial cathode (col. 4, lines 21-22), and where the coating materials are introduced into the region of the electrodes in a condensed state, such as a wire (col. 4, lines 15-17). Furthermore

Vukanovic et al states that suitable coating materials include silicon and other semiconductor component or dopant materials, such as aluminum (col. 4, lines 25-29). It is well known that an alloy comprises a mixture of two or more elements with at least one of the elements being a metal. Thus a coating material comprising silicon and aluminum is an aluminum alloy.

With respect to claim 15, Vukanovic et al further discloses suitable coating materials including aluminum and copper (col. 4, lines 25-33). Vukanovic et al states that "the temperature of the plasma jet which emerges from the exit orifice [...] has been measured from 200°C – 700°C" (col. 5, lines 42-44). The exit orifice [44] can be seen in fig. 3 near arc plasma region [16]. Fig. 4 depicts the arc plasma region adjacent to the substrate [43], as also stated (col. 8, lines 28-31). Thus the substrate is in close proximity to the exit orifice with the substrate layers being exposed to an energy source (i.e. the plasma jet heat). However Vukanovic et al is limited in that while it describes using these components for the coating materials, it is not suggested as to the specific compositional percentages of these components.

It has been held that differences in concentration or temperature will not support patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Therefore it would have been obvious to one of ordinary skill in the art to use the coating material composition discussed in Vukanovic et al with various percentage compositions, including those claimed, since one of ordinary skill would expect similar characteristics.

6. Claims 10-11 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vukanovic et al (US Patent No. 4,505,947) as applied to claims 7 and 12 above, and further in view of Wu et al (USPGPub 2003/0102207).

With respect to claims 10 and 11, the reference is cited as discussed for claim 7. Vukanovic et al further discloses suitable coating materials, including germanium. Vukanovic et al also discloses that the coating material may be placed on or in the cathode (col. 4, lines 4-6), such as a sacrificial cathode (col. 4, lines 21-22), and where the coating materials are introduced into the region of the electrodes in a condensed state, such as a wire (col. 4, lines 15-17). Furthermore Vukanovic et al states that suitable coating materials include silicon and other semiconductor component or dopant materials, such as aluminum and germanium (col. 4, lines 25-29). It is well known that an alloy comprises a mixture of two or more elements with at least one of the elements being a metal. Thus a coating material comprised of silicon, aluminum, and germanium is an alloy. However Vukanovic et al is limited in that while it discusses using a germanium alloy coating, it is not suggested to use a coating of selenium or tellurium

Wu et al teaches a similar apparatus for providing a chamber for collecting material (i.e. coating a substrate) generated from an electrically conductive starting material selected from a group consisting of a metal alloy, operating a twin-wire arc nozzle and a working gas flow to form an arc between two converging leading tips (i.e. electrodes) and at least partially vaporizing the starting material to provide a stream (i.e. plasma stream), where a gas is injected to direct the stream (abstract). Wu et al further teaches that the invention is applicable to a number of metals for starting materials,

including titanium, tantalum, tungsten, copper (p. 3, para 32), aluminum (p. 3, para 33) germanium (p. 3, para 35), selenium and tellurium (p. 4, para 37). It is known that selenium and tellurium are chalcogens.

Since the prior art of Wu et al recognizes the equivalency of germanium, selenium, and tellurium in the field of electrical arcing, it would have been obvious to one of ordinary skill in the art to replace germanium of Vukanovic et al with selenium and tellurium of Wu et al as it is merely the selection of functionally equivalent chalcogens recognized in the art and one of ordinary skill in the art would have a reasonable expectation of success in making the modification.

With respect to claims 16-17, the reference is cited as discussed for claim 12. Vukanovic et al further discloses suitable coating materials including silicon and germanium. Vukanovic et al also discloses that "the temperature of the plasma jet which emerges from the exit orifice […] has been measured from 200°C – 700°C" (col. 5, lines 42-44). The exit orifice [44] can be seen in fig. 3 near arc plasma region [16]. Fig. 4 depicts the arc plasma region adjacent to the substrate [43], as also stated (col. 8, lines 28-31). Thus the substrate is in close proximity to the exit orifice with the substrate layers being exposed to an energy source (i.e. the plasma jet heat). Furthermore it is well known that the melting point of aluminum (i.e. plurality of metal from claim 12) is below 700°C, thus aluminum melts and forms an interdiffused layer with the other components. However Vukanovic et al is limited in that while it discusses using a germanium coating, it is not suggested to use a coating of selenium or tellurium.

Wu et al teaches a similar apparatus for providing a chamber for collecting material (i.e. coating a substrate) generated from an electrically conductive starting material selected from a group consisting of a metal alloy, operating a twin-wire arc nozzle and a working gas flow to form an arc between two converging leading tips (i.e. electrodes) and at least partially vaporizing the starting material to provide a stream (i.e. plasma stream), where a gas is injected to direct the stream (abstract). Wu et al further teaches that the invention is applicable to a number of metals for starting materials, including titanium, tantalum, tungsten, copper (p. 3, para 32), aluminum (p. 3, para 33) germanium (p. 3, para 35), selenium and tellurium (p. 4, para 37). It is known that selenium and tellurium are chalcogens.

Since the prior art of Wu et al recognizes the equivalency of germanium, selenium, and tellurium in the field of electrical arcing, it would have been obvious to one of ordinary skill in the art to replace germanium of Vukanovic et al with selenium and tellurium of Wu et al as it is merely the selection of functionally equivalent chalcogens recognized in the art and one of ordinary skill in the art would have a reasonable expectation of success in making the modification.

7. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vukanovic et al (US Patent No. 4,505,947) as applied to claim 18 above, and further in view of Lee et al (US Patent No. 7,192,335).

With respect to claims 21-23, Vukanovic et al is limited in that a process after deposition, such as polishing, is not suggested.

Lee et al teaches a method for chemically, mechanically, and electrolytically removing material from substrates (abstract) with gaps (figs. 1-2). Lee et al discusses a method of engaging the substrate with a polishing pad (i.e. machining) and disposing a polishing liquid (i.e. cleaning solvent) adjacent to the polishing surface, with the polishing liquid containing about 1% abrasive particles (col. 2, lines 25-30). Since the polishing liquid contains a percentage of abrasive particles, the liquid removes some material thus cleaning the surface of the substrate. And since the polishing liquid follows the step of the polishing pad, the polishing liquid removes machining residue. Lee et al suggests that the polishing liquid be ammonium hydroxide (col. 2, lines 19-26), a well known cleaning solvent. Furthermore, Lee et al states moving at least one of the polishing pad and the substrate relative to the other to remove material from the substrate (col. 2, lines 34-37), thus machining the substrate to a predetermined thickness. Lee et al cites the advantage of polishing as a removal of excess conductive (i.e. copper and aluminum) material (col. 2, lines 51-54).

It would have been obvious to one of ordinary skill in the art to incorporate polishing the substrate as taught in Lee et al for the method of Vukanovic et al to gain the advantage of removing excess conductive material from the substrate.

Response to Arguments

<u>*Claim Objections*</u>

8. The minor informality in claim 18 has been amended. Therefore the objection is withdrawn.

112 Rejections

9. The Applicant has clarified what is meant by the term “chalcogenide”. Therefore the rejections to claims 10-11 and 17 are withdrawn. However the Examiner respectfully notes that an example provided by the Applicant of a given chalcogenide material as GeSb (germanium-antimony) is not a chalcogenide material as defined by the Applicant.

102 & 103 Rejections

10. On pages 12-13, the Applicant's argues that Vukanovic et al does not teach “providing the pre-sputtered surface of the target comprising the sputtered depression, in a process zone” in addition to “directing the liquefied metal into the sputtered depression of the target to at least partially fill the sputtered depression with liquefied metal”.

The Examiner respectfully disagrees. In regards to a “pre-sputtered surface of the target comprising the sputtered depression, in a process zone”, the Examiner has provided the following evidence: “Vukanovic et al further discloses that the coating material is deposited onto the surface of the substrate (col. 3, lines 8-13), where the substrate may be a semiconductor (col. 3, lines 14-23). While Vukanovic et al does not suggest the substrate (i.e. used target) have depressions or gaps (i.e. sputtered surfaces), it is either inherent or obvious that a semiconductor substrate (i.e. used target) possess this specified feature as evidenced by Miyazaki (US Patent No. 5,595,938; figs. 1-4) and Lee et al (US Patent No. 7,192,335; figs. 1-2). Furthermore it is

well known that a sputter target (i.e. substrate) is eroded unevenly during use, leading to depressions on the target surface”. In regards to directing liquefied metal into sputtered depression of the target, the Examiner has provided the following evidence: “Vukanovic et al further discloses that the coating material is deposited onto the surface of the substrate (col. 3, lines 8-13), where the substrate may be a semiconductor (col. 3, lines 14-23)” in addition, “Vukanovic et al further discloses that the coating material may be placed on or in a cathode, where it is vaporized by the heat of the cathode and carried into the plasma region by a carrier gas (col. 4, lines 4-9). Vukanovic et al describes how the coating materials are introduced into the region of the electrodes in a condensed state, such as a wire and volatized by the heat generated at or on the cathode (col. 4, lines 15-19) and if conductive (i.e. metal) as a sacrificial (i.e. consumable) cathode (col. 4, lines 19-22). Vukanovic et al lists suitable coating materials as metals (col. 4, lines 25-33). Vukanovic et al also describes how the plasma material is introduced into the arc plasma and positioning a substrate material proximate to the arc plasma, whereby said coating material formed by the arc plasma contact the substrate to form a coating (col. 3, lines 8-13). It is well known that for a solid to be vaporized, the solid transitions from a solid state to a liquid state, thus the metal is liquefied”. Furthermore, semiconductors are well known to have recesses, depressions, trenches, or channels which are filled to form the semiconductors wiring.

11. On pages 13-18, the Applicant argues that the 103 rejections based upon obviousness of Vukanovic et al and combinations of Wu et al and Lee et al with

Vukanovic et al are nonobvious since Vukanovic et al fails to teach the limitations of claim 1.

The Examiner respectfully disagrees. In regards to a “pre-sputtered surface of the target comprising the sputtered depression, in a process zone”, the Examiner has provided the following evidence: “Vukanovic et al further discloses that the coating material is deposited onto the surface of the substrate (col. 3, lines 8-13), where the substrate may be a semiconductor (col. 3, lines 14-23). While Vukanovic et al does not suggest the substrate (i.e. used target) have depressions or gaps (i.e. sputtered surfaces), it is either inherent or obvious that a semiconductor substrate (i.e. used target) possess this specified feature as evidenced by Miyazaki (US Patent No. 5,595,938; figs. 1-4) and Lee et al (US Patent No. 7,192,335; figs. 1-2). Furthermore it is well known that a sputter target (i.e. substrate) is eroded unevenly during use, leading to depressions on the target surface”. In regards to directing liquefied metal into sputtered depression of the target, the Examiner has provided the following evidence: “Vukanovic et al further discloses that the coating material is deposited onto the surface of the substrate (col. 3, lines 8-13), where the substrate may be a semiconductor (col. 3, lines 14-23)” in addition, “Vukanovic et al further discloses that the coating material may be placed on or in a cathode, where it is vaporized by the heat of the cathode and carried into the plasma region by a carrier gas (col. 4, lines 4-9). Vukanovic et al describes how the coating materials are introduced into the region of the electrodes in a condensed state, such as a wire and volatized by the heat generated at or on the cathode (col. 4, lines 15-19) and if conductive (i.e. metal) as a sacrificial (i.e.

consumable) cathode (col. 4, lines 19-22). Vukanovic et al lists suitable coating materials as metals (col. 4, lines 25-33). Vukanovic et al also describes how the plasma material is introduced into the arc plasma and positioning a substrate material proximate to the arc plasma, whereby said coating material formed by the arc plasma contact the substrate to form a coating (col. 3, lines 8-13). It is well known that for a solid to be vaporized, the solid transitions from a solid state to a liquid state, thus the metal is liquefied”. Furthermore, semiconductors are well known to have recesses, depressions, trenches, or channels which are filled to form the semiconductors wiring.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent No. 7,175,802; US Patent No. 6,635,219; US Patent No. 6,518,086; US Patent No. 6,409,965; US Patent No. 6,071,323

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Band whose telephone number is (571) 272-9815. The examiner can normally be reached on Mon-Fri, 8am-4pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexa Neckel can be reached on (571) 272-1446. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. B./

Examiner, Art Unit 1795

/Alexa D. Neckel/

Supervisory Patent Examiner, Art Unit 1795